< DE/EJ/ET/EN/EX/EQ/IE/IS/IC >: <22636>: <Emerging Trends in Electronics>: <Advance Processors>: <UO1b.2: Explain different blocks of ATmega 328 microcontroller >: <Assessments>: <Formative>

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| Set 1: Question No 1 | Set 1: Question No 2 | Set 1: Question No 3 |
| Program instructions are stored in \_\_\_\_\_\_\_\_\_\_ [memory](https://en.wikipedia.org/wiki/Flash_memory). | Function of JTAG port is | In Atmega 328p chip P refers to |
| Recall/ Remembering | Understanding | Application |
| 1. [non-volatile](https://en.wikipedia.org/wiki/Non-volatile) flash | 1. Fetch | 1. production |
| 1. volatile | 1. Debug | 1. pinmode |
| 1. primary storage | 1. Decode | 1. pico-power |
| 1. RAM | 1. Execute | 1. programmable on chip |
| Ans: < a > | Ans: < b > | Ans: < c > |

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| --- | --- | --- |
| Set 2: Question No 1 | Set 2: Question No 2 | Set 2: Question No 3 |
| The AVRs have \_\_\_\_ [single-byte](https://en.wikipedia.org/wiki/Byte) [registers](https://en.wikipedia.org/wiki/Processor_register) and are classified as 8-bit RISC devices. | Function of Data Direction Register is | Atmel's AVRs have a \_\_\_\_\_\_\_\_ |
| Recall/ Remembering | Understanding | Application |
| 1. 8 | 1. configures the pins as either inputs or outputs | 1. One-stage, double-level [pipeline](https://en.wikipedia.org/wiki/Pipeline_(computing)) design. |
| 1. 16 | 1. configures timer | 1. Four-stage, single-level [pipeline](https://en.wikipedia.org/wiki/Pipeline_(computing)) design. |
| 1. 32 | 1. configures counter | 1. Four-stage, four-level [pipeline](https://en.wikipedia.org/wiki/Pipeline_(computing)) design. |
| 1. 64 | 1. configures serial port | 1. Two-stage, single-level [pipeline](https://en.wikipedia.org/wiki/Pipeline_(computing)) design. |
| Ans: < c > | Ans: < a > | Ans: < d > |